wherein said control circuit refers to said erase table for search of a memory area to which rewrite data is written, and

wherein said control circuit is adapted to store into a predetermined area of said nonvolatile memory an updated version of the erase table, which includes an updated free-space information flag from a previous version of the erase table, the predetermined area being a different area than an area in which the previous version of the erase table is stored.

2. (Currently Amended) A memory card comprising:

an nonvolatile memory; and a control circuit,

wherein said nonvolatile memory has, in a part of a memory array, an erase table in which a free-space information flag is associated with each physical address of a memory area,

wherein said free-space information flag has one of a first status and a second status,

wherein said first status is indicating that the corresponding memory area is permitted to be erased and said second status indicating that the corresponding memory area is inhibited to be erased, ~~and~~

wherein said control circuit uses a first physical address according to the free-space information flag in the first status obtained by searching said erase table as a memory area to which rewrite data is written, and

wherein said control circuit is adapted to store into a predetermined area of said nonvolatile memory an updated version of the erase table, which includes an updated free-space information flag from a previous version of the erase table, the predetermined area being a different area than an area in which the previous version of the erase table is stored.

3. (Currently Amended) A memory card comprising:

nonvolatile memory; and a control circuit,

wherein a memory array of said nonvolatile memory has an erase table and an address translation table, wherein a free-space information flag in said erase table is associated with each physical address of a memory area, wherein a physical address of a memory area in said address translation table is associated with each logical address, wherein said free-space information flag indicates whether a corresponding memory area is permitted to be erased or not, ~~and~~

wherein said control circuit determines a physical address of a memory area to which rewrite data is written by referring to the free-space information flag of said erase table, updates the address translation table by associating the physical address of the memory area with the logical address and updates the free-space information flag of the erase table, and

wherein said control circuit is adapted to store into a predetermined area of said nonvolatile memory an updated version of the erase table, which includes an updated free-space information flag from a previous version of the erase table, the predetermined area being a different area than an area in which the previous version of the erase table is stored.

4. (Currently Amended) The memory card according to claim 3, wherein said erase table is stored into a plurality of memory areas each of which is arranged to different erase units, and wherein a first erase table is referred to when a memory area to which rewrite data is written is determined,

wherein a second erase table ~~is held~~stores a free space information flag according to a second memory area in which data to be rewritten, and

wherein said first erase table is formed in a memory area having an erase unit different from a second erase unit of the second erase table.

5. (Previously Presented) The memory card according to claim 4, wherein processes of updating the free-space information flag of the erase table includes a first updating process of making a first free-space information flag in said first erase table corresponding to said first memory area to an erase inhibited status, and a second updating process of making a second free-space information flag in said second erase table corresponding to said second memory area to an erase permitted status.

6. (Previously Presented) The memory card according to claim 5, wherein said first updating process is performed and, after that, the second updating process is performed.

7. (Previously Presented) The memory card according to claim 6, wherein a process of updating an address translation table by associating a logical address and a physical address of said first memory area to which said data has been written with each other is performed between said first and second updating processes.

8. (Currently Amended) The memory card according to claim 7, wherein the erase table is disposed so as to be divided into a plurality of memory areas, each of said memory areas is assigned to different erase units, is multiplexed on the memory areas, and the multiplexed erase tables are sequentially updated and used so as to alternately change the erase unit.

9. (Previously Presented) The memory card according to claim 8, wherein said address translation table is arranged so as to be divided into a plurality of memory areas, each of said memory areas is assigned to different erase units, is multiplexed on the memory areas, and the multiplexed address translation tables are sequentially updated so as to alternately change the erase unit.

10. (Previously Presented) The memory card according to claim 3, wherein said control circuit searches said address translation table for a memory area from which data is read.

11. (Previously Presented) The memory card according to claim 3, wherein the erase unit of said nonvolatile memory is larger than a write unit instructed from the outside.

12. (Previously Presented) A memory card comprising:

nonvolatile memory; and a control circuit,

wherein a memory array of said nonvolatile memory has an erase table and an address translation table,

wherein a free-space information flag in said erase table is associated with each physical address of a memory area and said free-space information flag indicateswhether the corresponding memory area is permitted to be erased or not,

wherein a physical address of a memory area in said address translation table is associated with each logical address, and

wherein, at the time of rewriting stored information, said control circuit reads an address translation table corresponding to a logical address to be rewritten into a buffer, obtains a physical address of rewrite data from the read address translation table, reads a first memory area of the obtained physical address, stores the read data into the buffer, reads a first erase table corresponding to said obtained physical address into the buffer, reads a second erase table used to retrieve a second memory area to which rewrite data is written into the buffer, determines said second memory area to which rewrite data is written by

referring to a free-space information flag of said second erase table, merges said stored data with data which is input from the outside, writes said merged data as rewrite data into said determined memory area, updates a correspondence between the physical address of said second memory area and the logical address on the address translation table read into the buffer, updates the free-space information flag on the first erase table and said second erase table read into the buffer, and writes the updated erase table and the updated address translation table into a flash memory.

13. (Previously Presented) The memory card according to claim 12, wherein the process of writing the updated erase table and the address translation table into the flash memory is performed in accordance with an order of the second erase table, the address translation table, and the first erase table.

14. (Previously Presented) The memory card according to claim 13, wherein the erase table is disposed so as to be divided into a plurality of memory areas, each of said memory areas is assigned to different erase units, is multiplexed on the memory areas, and the multiplexed erase

tables are sequentially updated and used so as to alternately change the erase unit.

15. (Previously Presented) The memory card according to claim 14, wherein said address translation table is arranged so as to be divided into a plurality of memory areas, each of said memory areas is assigned to different erase units, is multiplexed on the memory areas , and the multiplexed address translation tables are sequentially updated so as to alternately change the erase unit.

16. (Currently Amended) A memory card comprising an nonvolatile memory,

wherein said nonvolatile memory includes, in a part of a memory array, an erase table in which a free-space information flag is associated with each physical address of a memory area and an address translation table in which a physical address of the memory area is associated with each logical address,

wherein said free-space information flag has a first status indicating that the corresponding memory area is permitted to be erased and a second status indicating that the corresponding memory area is inhibited to be erased, ~~and~~

wherein a memory area to which rewrite data is to be written is determined by a physical address according to the free-space information flag in the first status retrieved, and

wherein an updated version of the erase table, which includes an updated free-space information flag from a previous version of the erase table, is stored into a predetermined area of said nonvolatile memory, the predetermined area being a different area than an area in which the previous version of the erase table is stored.

17. (Previously Presented) The memory card according to claim 16,

wherein said erase table is disposed so as to be divided into a plurality of memory areas each of which assigned to different erase units,

wherein a first erase table is referred to when a first memory area to which rewrite data is written is determined,

wherein a second erase table is held a free-space information flag according to a second memory area in which data to be rewritten,

wherein said first erase table is formed in a memory area having a first erase unit different from a second erase unit of the second erase table, and

wherein the second memory area is determined with reference to the address translation table.